TETRACOM: Technology Transfer in Computing Systems

FP7 Coordination and Support Action to fund 50 technology transfer projects (TTP) in computing systems. This project has received funding from the European Union's Seventh Framework Programme for research, technological development and demonstration under grant agreement n° 609491.

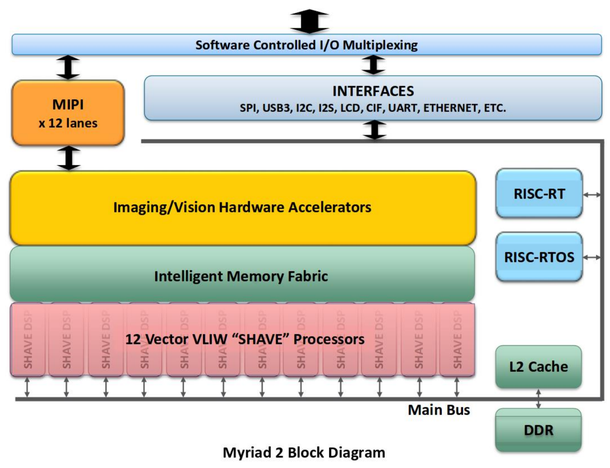
High-speed Instruction Set Simulator for Movidius SHAVE Core

Jakub Kaszyk, Björn Franke, University Of Edinburgh, UK
Claudiu Steflea, Alin Dobre, Brendan Barry, Movidius, USA

TTP Problem

The **Myriad-2** system-on-chip (SoC) is designed for high performance, low-power computational imaging and visual awareness applications in power-constrained mobile, wearable, and embedded devices. The video processing is accelerated by 12 VLIW **SHAVE** processors, which we aim to simulate.

Goals:
To develop a high speed instruction set simulator to aid in the design of a high-performance, ultra-low power programmable architecture with a small-area footprint.



Myriad 2 Block Diagram

Problems:
- Complex Architecture that is difficult to simulate
- Long Processor Design Cycle
- Costly Processor Design Cycle
- Difficult to test
- Long Development time for handwritten simulator

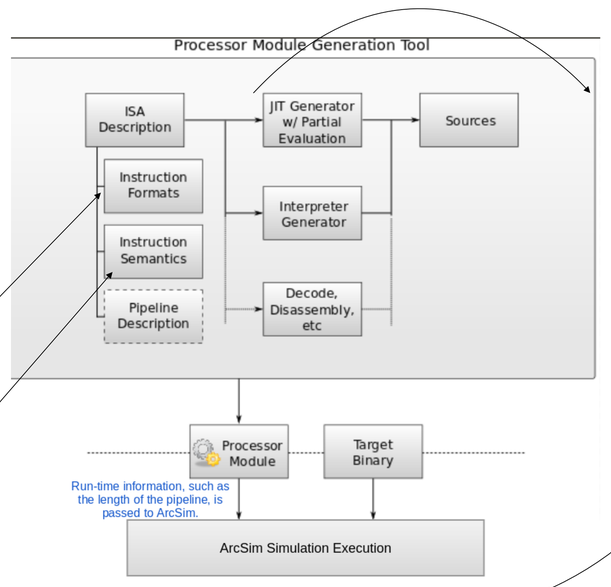
Existing solutions:
- Slow RTL Simulation
- Slow Proprietary Simulation

TTP Solution

Auto-Generation of High Speed Instruction Set Simulator

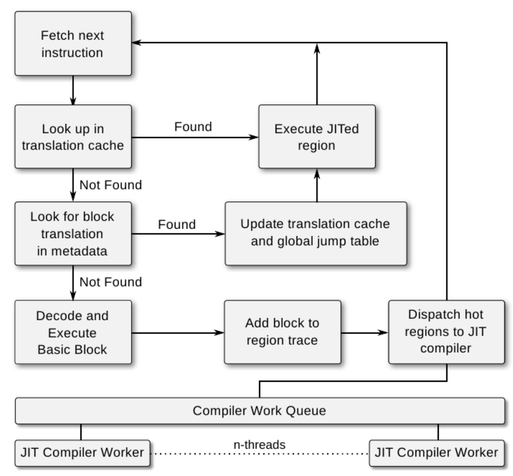
Arcsim and **Gensim** form a High-Speed Simulation and Automatic Generation Framework. Arcsim and Gensim were modified to support automatic generation of a High Speed Simulator with JIT DBT from an ArchC description of the Architecture.

Customized decoder generator, modified backend for VLIW Generation



Generated Gensim Processor Module is plugged into Arcsim

Optimized JIT DBT backend with support for VLIW architectures delivers excellent performance results.



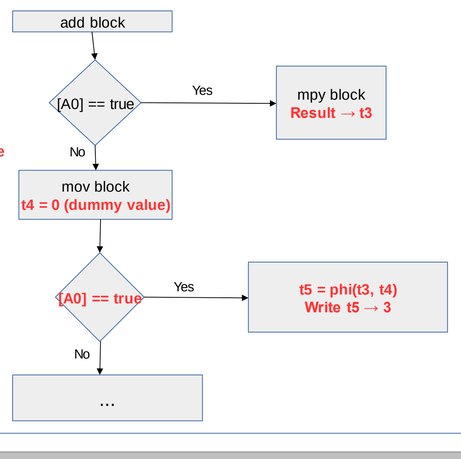
ArchC Model Parsed By Gensim

```
/* Decode Format */
ac_format Type_S1 =
  "%cond:4 %dst:5 %src2:5 %src1cst:5 %x:1 %op:6 %subop:4 %s:1 %p:1";

/* Instructions with specified decode format */
ac_instr<Type_S1> b, birp;

/* Static fields in decoding for birp instruction */
birp.set_decoder(src2=0x6, op=0x3, subop=0x8);

/* Instruction Disassembly */
birp.set_asm("%cond birp .S%unit IRP %prll", cond, uf, p);

/* Features enabling JIT optimisation */
birp.set_behaviour(birp);
birp.set_end_of_block();
birp.set_variable_jump();
birp.set_delayed_branch();

/* Instruction Behaviour */
execute(birp)
{
  uint32 irp;
  irp = read_register_bank(CRF, 6);
        write_register_bank_delayed(CRF,9,irp,6);
}
```

Modified JIT compiler to handle delayed effects

```
l1: add r2, r3, r4
 [A0] mpy r1, r2, t3
    mov r2, r4, r5
    write t3-> r3
```

Preserve pointer to old A0 value



TTP Impact

Auto-generated High-Speed Instruction Set Simulator → Fast, cost-effective design cycle → Efficient and Effective Processors with VLIW Cores

Advanced Visual Applications

- **Wearables** — Ultra-low power performance for compact wearables
- **Augmented & Virtual Reality** — Immersive digital worlds meeting reality
- **Robotics** — Visually intelligent robots
- **Smart Security** — Smarter, personalized security systems

TTP Facts

Contact: Björn Franke
E-mail: branke@inf.ed.ac.uk
TETRACOM contribution: 50,000 €
Duration: 01/06/2015-31/03/2016