TETRACOM: Technology Transfer in Computing Systems

FP7 Coordination and Support Action to fund 50 technology transfer projects (TTP) in computing systems. This project has received funding from the European Union's Seventh Framework Programme for research, technological development and demonstration under grant agreement n° 609491.

A Highly Optimized Arithmetic Software Library and Hardware Co-processor IP for Fixed-Point VLIW-SIMD Processor Architectures

Lukas Gerlach, Stephan Nolting, Holger Blume and Guillermo Payá Vayá, Leibniz Universität Hannover, Germany
Hans-Joachim Stolberg and Carsten Reuter, videantis GmbH, Hannover, Germany

TTP Problem

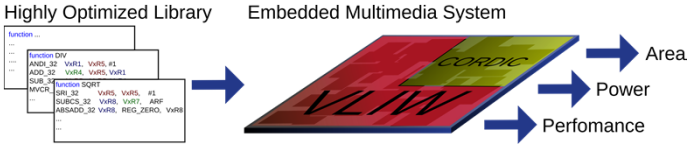
Performance requirements are pushing the limits of embedded multimedia systems:

Often used non-linear complex mathematical functions require a lot of **computational power**.

sin() atan() ln() div() cos() sqrt() exp() pow()

Area and energy efficiency is restricted for embedded multimedia systems:

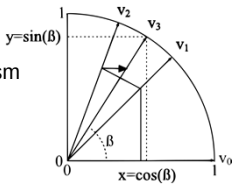
Area and energy optimized computation by using specific ***arithmetic evaluation software libraries*** or **hardware accelerators**.



TTP Solution

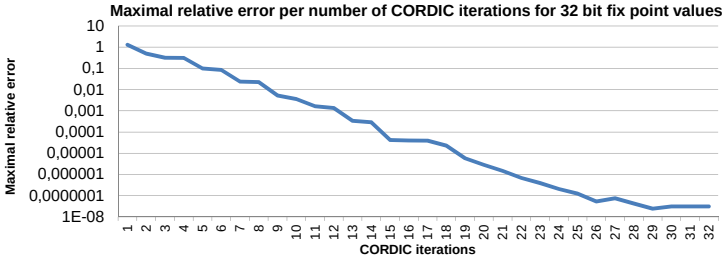
Software-based solution:

Mathematic software **CORDIC** (Coordinate Rotation Digital Computer) **library** (*LibARITH*)



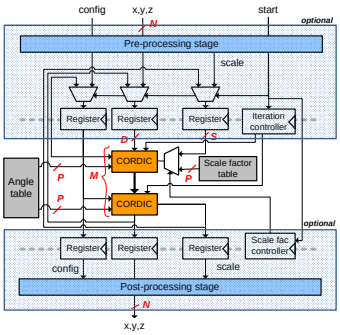
Optimized for VLIW-SIMD processors:
- Exploiting data and instruction level parallelism

Advantages:
- High flexibility
- High accuracy
- Fast computation compared to other approximation algorithms
- Reduced memory requirement compared to look-up-table interpolation



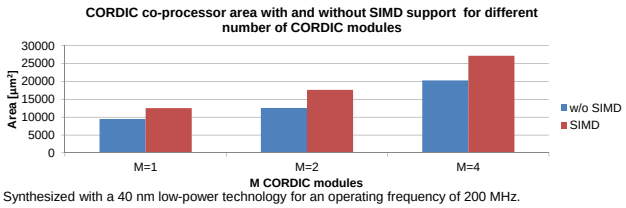
Hardware-based solution:

CORDIC processing element



Scalable co-processor architecture:
- M CORDIC modules in series are incorporated to process M CORDIC iterations per clock cycle

Data level parallelism (SIMD) is supported.



Synthesized with a 40 nm low-power technology for an operating frequency of 200 MHz.

TTP Impact

Hyperbolic and trigonometric operations (32-bit)			sin()	cos()	atan()	div()	exp()	ln()	sqrt()	pow()
Cycles	HW	VLIW-SIMD+CORDIC w/o SIMD	55+30+32+18 (*) =135	55+30+32+18 (*) =135	55+10+32+5 (*) =102	55+17+32+9 (*) =113	55+28+32+17 (*) =121	55+15+32+12 (*) =114	55+18+32+9 (*) =114	51+49+32+27 (*) =159
	SW	VLIW-SIMD (SW CORDIC)	55+30+408+53 (*) =546	55+30+408+18 (*) =511	55+10+408+5 (*) =478	55+17+408+9 (*) =489	55+28+408+17 (*) =508	55+15+408+12 (*) =490	55+18+408+9 (*) =490	51+49+408+27 (*) =535
	SW	TI TMS320C6748	2474	1423	3759	152	2557	2721	311	4176

(*) Notation for VLIW: table-configuration + pre-processing + CORDIC-core-iterations + post-processing

- The CORDIC-co-processor with SIMD support computes multiple independent results within the same number of CORDIC-core-iterations.
- The number of CORDIC modules linearly decreases the needed number of CORDIC-core-iteration cycles for the same precision.
- The area of the CORDIC co-processor without SIMD accounts for about 7% of the area of a reference VLIW-SIMD processor architecture.

TTP Facts

Contact: Jun.-Prof. Dr.-Ing. Guillermo Payá Vayá
E-mail: guipava@ims.uni-hannover.de
TETRACOM contribution: 25.000 €
Duration: 1/1/2016-31/7/2016

videantis passion for video

Leibniz Universität Hannover